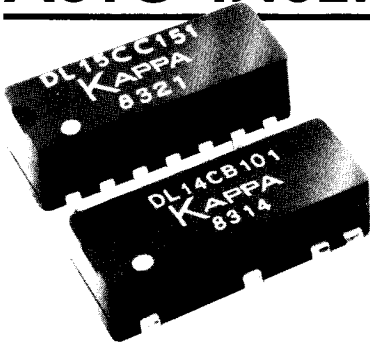


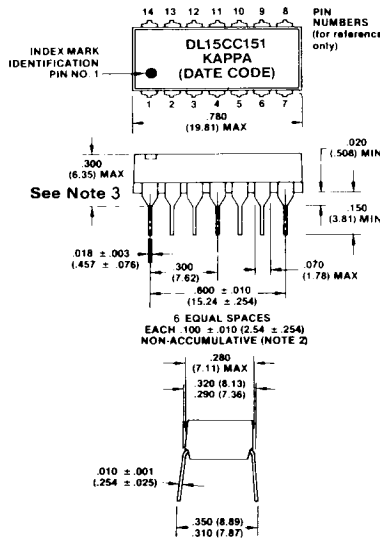
SERIES DL14/DL15 TTL SCHOTTKY (14-PIN) 5-TAP/10-TAP AUTO-INSERTABLE DELAY LINES



FEATURES

- Auto-Insertable 14-pin package
- TTL Schottky interfaced
- 5/10 equally spaced taps
- Risettime: 4 ns max⁽⁵⁾ ⁽⁶⁾
- Total delays from 25-500 ns

MARKINGS AND DIMENSIONS, in (mm)



Marking and dimension notes:

1. A notch may be substituted for PIN #1 Dot Index.
2. Each terminal is located within ± 0.10 of its nominal multiple of .400 along this longitudinal dimension relative to terminals 7 and 8.
3. Also available in .200 in. max mounting height as DL14CA and .165 in. max mounting height as DL14CZ.

RECOMMENDED OPERATING CONDITIONS

| | MIN | TYP | MAX | UNIT |
|---|------|------|------|------|
| V _{CC} Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V _{IH} High-Level Input Voltage | 2.0 | | | V |
| V _{IL} Low-Level Input Voltage | | | 0.8 | V |
| I _{IK} Input Clamp Current | | | -18 | mA |
| I _{OH} High-Level Output Current | | | -1.0 | mA |
| I _{OL} Low-Level Output Current | | | 20 | mA |
| T _A Operating Free-Air Temperature | 0 | +25 | +70 | °C |

DC ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

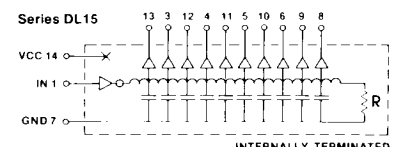
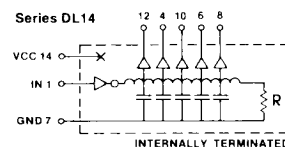
| Parameter | Test Conditions | MIN | TYP | MAX | UNIT |
|--|---|-----|--------|--------|----------|
| V _{OH} High-Level Output Voltage | V _{CC} = min, V _{IH} = min, I _{OH} = max | 2.7 | 3.4 | | V |
| V _{OL} Low-Level Output Voltage | V _{CC} = min, V _{IL} = max, I _{OL} = max | | | 0.5 | V |
| V _{IK} Input Clamp Voltage | V _{CC} = min, I _I = I _{IK} | | | -1.2 | V |
| I _{IH} High-Level Input Current | V _{CC} = max, V _{IN} = 2.7V | | | 50 | μA |
| | V _{CC} = max, V _{IN} = 5.25V | | | 1.0 | mA |
| I _{IL} Low-Level Input Current | V _{CC} = max, V _{IN} = 0.5V | | | -2 | mA |
| I _{OS} Short Circuit Output Current | V _{CC} = max, V _{OUT} = 0, one output at a time | -40 | | -100 | mA |
| I _{CC} H High-Level Supply Current | V _{CC} = max, V _{IN} = OPEN | | 30/60 | 45/75 | mA |
| I _{CC} L Low-Level Supply Current | V _{CC} = max, V _{IN} = 0 | | 65/120 | 75/150 | mA |
| N _H Fanout High-Level Output | V _{CC} = max, V _{OH} = 2.7V | | | 20 | TTL load |
| N _L Fanout Low-Level Output | V _{CC} = max, V _{OL} = 0.5V | | | 10 | TTL load |

INPUT PULSE TEST CONDITIONS

| Parameter | 3.1 | 3.2 | 3.3 | V |
|--|-------|------|-----|----|
| E _{IN} Pulse Voltage | | | | V |
| T _{RI} Pulse Rise-Time | | | 2.0 | ns |
| T _W Pulse Width, of Total Delay | 40/20 | 100 | | % |
| d Duty Cycle | | 33.3 | 50 | % |

| PART NUMBER | Total Delay (ns) ⁽¹⁾ ⁽²⁾ | Tap Delay (ns) ⁽¹⁾ ⁽²⁾ | Notes: |
|-------------|--|--|--|
| DL14CB250 | 25 | 5 | 1. Delays measured at 1.5V level on leading edge only. 2. Delay tolerances: $\pm 5\%$ or ± 2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: V _{CC} = T _{yp} , T _A = T _{yp} , E _{IN} = T _{yp} , T _{RI} = max, T _W = T _{yp} , P _{RR} = 1MHz (or d/tw, whichever is less), R _L 1 megohm and C _L 2 pf. 3. Temperature coefficient of delay will vary, depending upon total delay, according to the formula: T _{PTA} = (100 + (25,000/T _{PLH})). 4. Delay will vary approximately 4% for every 5% change in supply voltage. 5. Risettime measured from 0.75V to 2.4V level. 6. Measured with no loads on taps. 7. Other delays also available upon request. 8. Typical trailing edge delay = leading edge delay within $\pm 15\%$ typ. |
| DL14CB500 | 50 | 10 | |
| DL14CB750 | 75 | 15 | |
| DL14CB101 | 100 | 20 | |
| DL14CB251 | 250 | 50 | |
| DL14CB501 | 500 | 100 | |
| DL15CC500 | 50 | 5 | |
| DL15CC101 | 100 | 10 | |
| DL15CC151 | 150 | 15 | |
| DL15CC201 | 200 | 20 | |
| DL15CC251 | 250 | 25 | |
| DL15CC501 | 500 | 50 | |

FIGURE 1 — SCHEMATIC



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